L Number	Hits	Search Text	DB	Time stamp
1	2820	438/627,637,643,653.ccls. and @ad<20020102	USPAT; US-PGPUB	2004/07/22 15:24
2	44	(438/627,637,643,653.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)	USPAT; US-PGPUB	2004/07/22 15:25
3	2409	438/672,675,700,724,761.ccls. and @ad<20020102	USPAT; US-PGPUB	2004/07/22 15:29
4	20	(438/672,675,700,724,761.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)	USPAT; US-PGPUB	2004/07/22 15:29
5	11	((438/672,675,700,724,761.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)) not ((438/627,637,643,653.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier))	USPAT; US-PGPUB	2004/07/22 15:25
6	2346	438/634,687,688,706.ccls. and @ad<20020102	USPAT; US-PGPUB	2004/07/22 15:33
7	39	(438/634,687,688,706.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)	USPAT; US-PGPUB	2004/07/22 15:30
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9	24	(((438/634,687,688,706.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)) not (((438/672,675,700,724,761.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)) not ((438/627,637,643,653.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier)))) not ((438/627,637,643,653.ccls. and @ad<20020102) and ((silicon adj carbide) with barrier))	USPAT; US-PGPUB	2004/07/22 15:30

DOCUMENT-IDENTIFIER: US 20030089992 A1

TITLE: **SILICON CARBIDE** DEPOSITION FOR USE AS A **BARRIER** LAYER AND AN ETCH STOP

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Abstract Paragraph - ABTX (1):

The present invention generally provides an improved process for depositing **silicon carbide,** using a silane-based material with certain process parameters, onto an electronic device, such as a semiconductor, that is useful for forming a suitable **barrier** layer, an etch stop, and a passivation layer for IC applications. As a **barrier** layer, in the preferred embodiment, the particular **silicon carbide** material is used to reduce the diffusion of copper and may also used to minimize the contribution of the **barrier** layer to the capacitive coupling between interconnect lines. It may also be used as an etch stop, for instance, below an intermetal dielectric (IMD) and especially if the IMD is a low k, silane-based IMD. In another embodiment, it may be used to provide a passivation layer, resistant to moisture and other adverse ambient conditions. Each of these aspects may be used in a dual damascene structure.

Application Filing Date - APD (1):

19981001

Current US Classification, US Secondary Class/Subclass - CCSR (9):

438/634

Current US Classification, US Secondary Class/Subclass - CCSR (10):

438/687

Title - TTL (1):

SILICON CARBIDE DEPOSITION FOR USE AS A **BARRIER** LAYER AND AN ETCH STOP

Summary of Invention Paragraph - BSTX (2):

[0001] The present invention relates generally to the fabrication of integrated circuits on substrates. More particularly, the invention relates to a low temperature method for producing a **silicon carbide** film utilizing alkyl silanes under certain process regimes, which may be useful as a **barrier** layer, etch stop, and passivation layer.

Summary of Invention Paragraph - BSTX (10):

[0008] Therefore, there is a need for an improved process using **silicon carbide as a barrier** layer, an etch stop, and a passivation layer for ICs.

Summary of Invention Paragraph - BSTX (12):

[0009] The present invention generally provides an improved process for depositing **silicon carbide,** using a silane-based material with certain process parameters, onto an electronic device, such as a semiconductor, that is useful for forming a suitable **barrier** layer, an etch stop, and a passivation layer for IC applications. As a **barrier** layer, in the preferred embodiment, the particular **silicon carbide** material is used to reduce the diffusion of copper and may also used to minimize the contribution of the **barrier** layer to the capacitive coupling between interconnect lines. It may also be used as an etch stop, for instance, below an intermetal dielectric (IMD) and especially if the

IMD is a low k, silane-based IMD. In another embodiment, it may be used to provide a passivation layer, resistant to moisture and other adverse ambient conditions. Each of these aspects may be used in a dual damascene structure.

Summary of Invention Paragraph - BSTX (13):

[0010] A preferred process sequence for forming a **silicon carbide barrier** layer on a substrate, comprises introducing silicon, carbon, and a noble gas into a reaction zone of a process chamber, initiating a plasma in the reaction zone, reacting the silicon and the carbon in the presence of the plasma to form **silicon carbide,** and depositing a **silicon carbide barrier** layer on a substrate in the chamber. Another sequence comprises introducing silicon, carbon, and a noble gas in a reaction zone of a chamber, initiating a plasma in the reaction zone, reacting the silicon and the carbon in the presence of the plasma to form silicon carbide, and depositing a silicon carbide passivation layer on the substrate. Still another aspect may include a substrate having a **silicon carbide barrier** layer, comprising a semiconductor substrate, a dielectric layer deposited on the substrate, and a **silicon carbide barrier** layer having a dielectric constant of about 6 or less.

Detail Description Paragraph - DETX (18):

[0032] In addition to serving as an improved barrier/etch stop layer, the SiC films of the present invention may also be used as a passivation layer. The passivation layer may play an increasingly larger role in copper-based devices, because the copper diffuses into surrounding layers. Furthermore, the **silicon carbide** material, with some process modifications compared to the most preferred parameters of the **barrier**/etch stop material,